



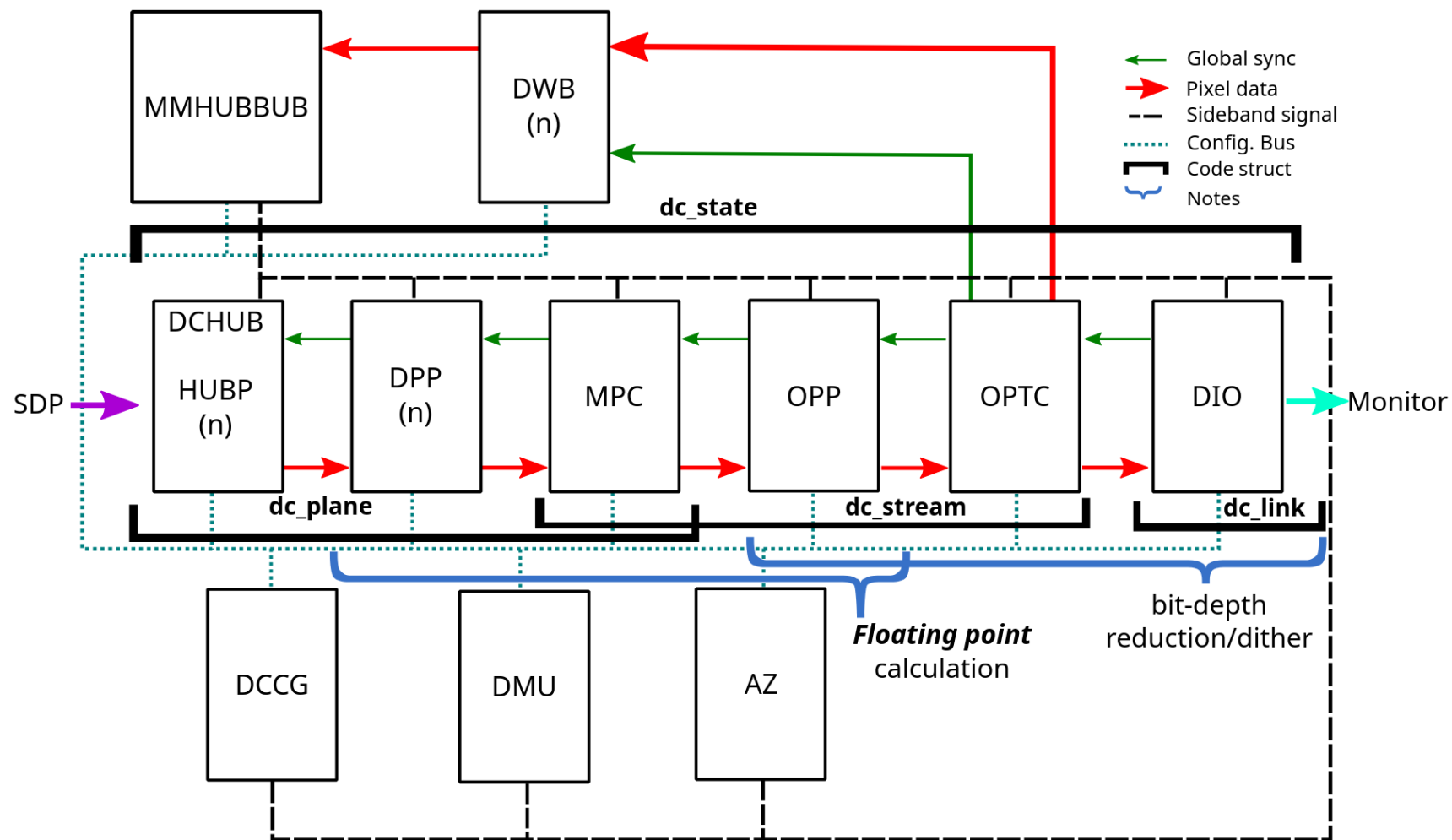
How do you debug and triage AMD display driver issues?

Rodrigo Siqueira



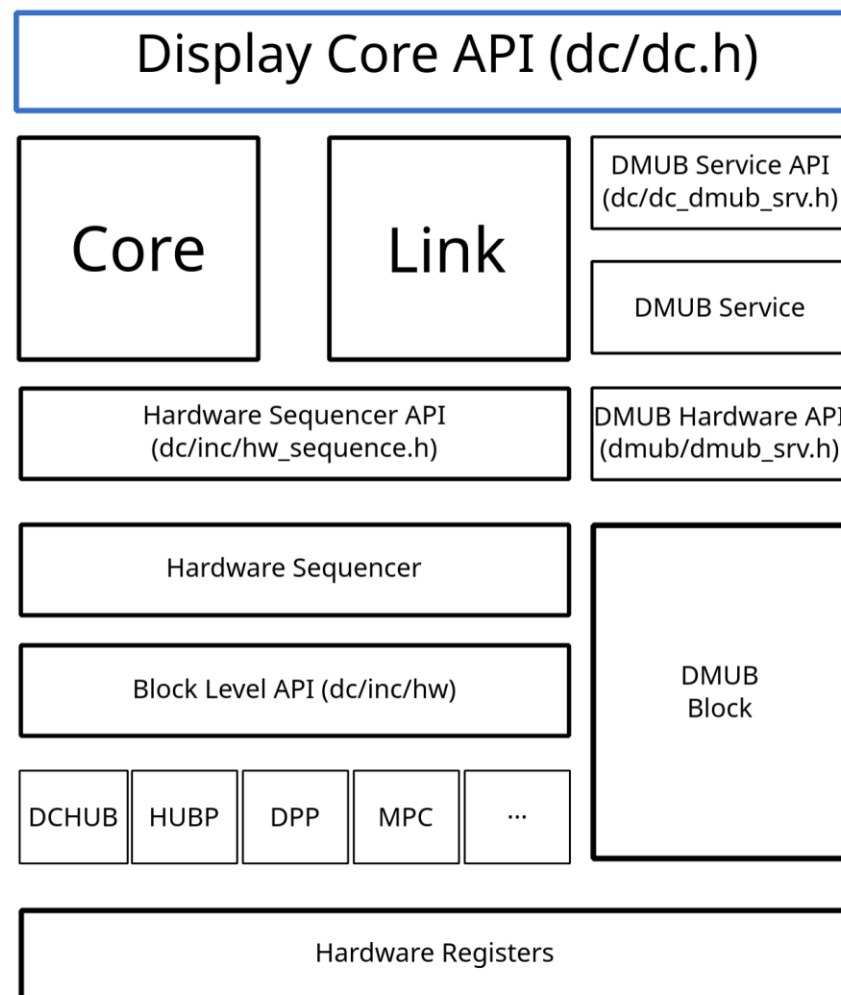
DCN Overview

DCN Overview



Ref: <https://www.kernel.org/doc/html/latest/gpu/amdgpu/display/dcn-overview.html>

DCN Overview





First Triage

Identify the DCN Version

```
amdgpu 0000:03:00.0: amdgpu: use vbios provided pptable  
amdgpu 0000:03:00.0: amdapu: SMU is initialized successfully!  
[drm] Display Core v3.2.303 initialized on DCN 3.0  
[drm] DP-HDMI FRL PCON supported  
[drm] DMUB hardware initialized: version=0x02020020  
[drm] kiq ring mec 2 pipe 1 q 0  
amdgpu: HMM registered 16368MB device memory  
kfd kfd: amdgpu: Allocated 3969056 bytes on gart  
kfd kfd: amdgpu: Total number of KFD nodes to be created: 1  
amdgpu: Virtual CRAT table created for GPU  
amdgpu: Topology: Add dGPU node [0x73bf:0x1002]
```

Load Component

```
[drm] initializing kernel modesetting (SIENNA_CICHLID 0x1002:0x73BF 0x1DA2:0x439E 0xC1).  
[drm] register mmio base: 0xFCC00000  
[drm] register mmio size: 1048576  
[drm] add ip block number 0 <nv_common>  
[drm] add ip block number 1 <gmc_v10_0>  
[drm] add ip block number 2 <navi10_ih>  
[drm] add ip block number 3 <psp>  
[drm] add ip block number 4 <smu>  
[drm] add ip block number 5 <dm>  
[drm] add ip block number 6 <gfx_v10_0>  
[drm] add ip block number 7 <sdma_v5_2>  
[drm] add ip block number 8 <vcn_v3_0>  
[drm] add ip block number 9 <jpeg_v3_0>
```

Disable DC – Post DCN 3.2 Method

Command line: `BOOT_IMAGE=/boot/vmlinuz-6.10.0-ASDN-SEPT-25+ root=UUID=a5acb1b6-dd07-4416-bad4-cab14efc1ec3 ro quiet splash vt.handoff=7 amdgpu.ip_block_mask=0xffffffff`

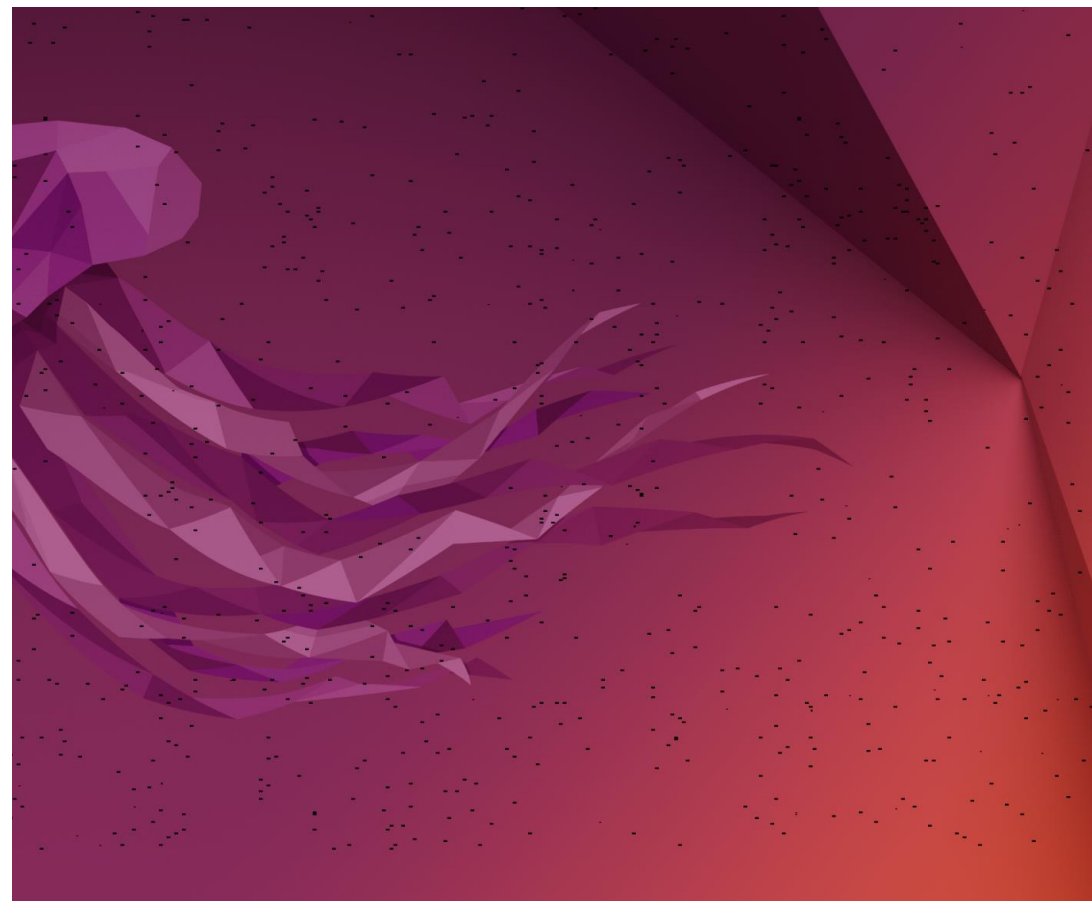
```
amdgpu 0000:03:00.0: enabling device (0000 - 0007)
[drm] initializing kernel modesetting (SIENNA_CICHLID 0x1002:0x73BF 0x1DA2:0x439E 0xC1).
[drm] register mmio base: 0xFCC00000
[drm] register mmio size: 1048576
[drm] add ip block number 0 <nv_common>
[drm] add ip block number 1 <gmc_v10_0>
[drm] add ip block number 2 <navi10_ih>
[drm] add ip block number 3 <psp>
[drm] add ip block number 4 <smu>
[drm] add ip block number 5 <dm>
[drm] add ip block number 6 <gfx_v10_0>
[drm] add ip block number 7 <sdma_v5_2>
[drm] add ip block number 8 <vcn_v3_0>
[drm] add ip block number 9 <jpeg_v3_0>
amdgpu 0000:03:00.0: amdgpu: Fetched VBIOS from VFCT
amdgpu: ATOM BIOS: 113-1E4392U-05H
[drm] disabled ip block: 5 <dm>
```

amdgpu.ip_block_mask=0xffffffff

$$0xffffffff \& \sim(1 \ll 5) = 0xffffffff$$

User Space Vs. Kernel Space Issues

- Take a screenshot or record the current desktop.
- Do you see the issue in the data collected?
- **Yes**: Invest more time in debugging the user space.
- **No**: The bug's origin is still inconclusive, which means you should keep working on the driver side.



Report the issue

New Issue

Title (required)

Type [?](#)

Issue ▼

Description

drm_BUG_TEMPLATE ▼

Preview | **B** *I* ~~S~~ | |

```
### Before submitting your bug report:  
  
< TODO: Drop this section >  
  
- Check if your bug has already been reported [here](lspci -nn | grep VGA).  
- For any logs, backtraces, etc - use [code blocks](https://docs.gitlab.com/ee/user/markdown.html#code-spans-and-blocks)  
- As examples of good bug reports you may review one of these - #1698, #1536, #1734  
  
Otherwise, fill the requested information below.  
And please remove anything that doesn't apply to keep things readable :)
```

Ref: <https://gitlab.freedesktop.org/drm/amd/-/issues/new>



**Narrow down the issue and
collect information**

From DC to Specific Parts of the Code

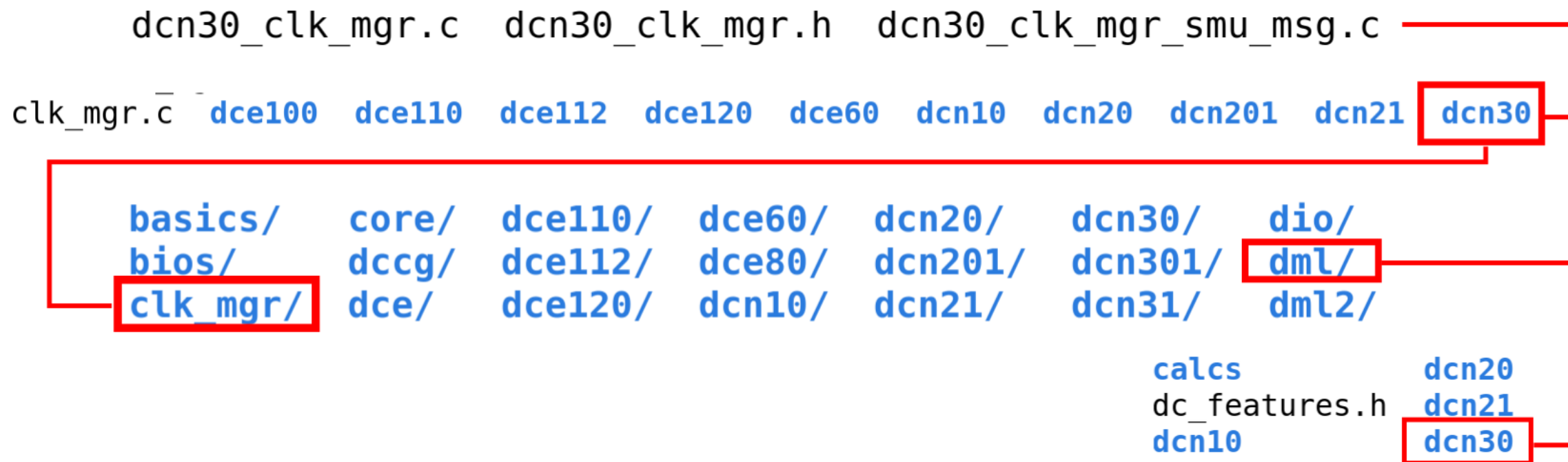
```
amdgpu 0000:03:00.0: amdgpu: use vbios provided pptable  
amdgpu 0000:03:00.0: amdgpu: SMU is initialized successfully!  
[drm] Display Core v3.2.303 initialized on DCN 3.0  
[drm] DP-HDMI FRL PCON supported  
[drm] DMUB hardware initialized: version=0x02020020  
[drm] kiq ring mec 2 pipe 1 q 0  
amdgpu: HMM registered 16368MB device memory  
kfd kfd: amdgpu: Allocated 3969056 bytes on gart  
kfd kfd: amdgpu: Total number of KFD nodes to be created: 1  
amdgpu: Virtual CRAT table created for GPU  
amdgpu: Topology: Add dGPU node [0x73bf:0x1002]
```

DCN Version: DCN_30

DC version: 3.2.303

Commit: drm/amd/display: 3.2.303

From DC to Specific Parts of the Code



Checking AMDGPU Events

```
amdgpu_dm_atomic_update_cursor: plane_id=88 plane_type=2 plane_state=000000001fda0796 state=00000000fa6befad crtc_id=91 fb(id=166 fmt=AR24 planes=1 mod=0) fence=0000000000000000 crtc_x=605 crtc_y=283  
lor range=0 visible=0
```

```
amdgpu_refresh_rate_track: crtc_index=0 refresh_rate=145Hz (6896289)  
amdgpu_refresh_rate_track: crtc_index=0 refresh_rate=48Hz (20831330)
```

- 1 amdgpu_dc_performance
- 2 amdgpu_dc_rreg
- 3 amdgpu_dc_wreg
- 4 amdgpu_dm_atomic_check_begin
- 5 amdgpu_dm_atomic_check_finish
- 6 amdgpu_dm_atomic_commit_tail_begin
- 7 amdgpu_dm_atomic_commit_tail_finish
- 8 amdgpu_dm_atomic_state_template
- 9 **amdgpu_dm_atomic_update_cursor**
- 10 amdgpu_dm_connector_atomic_check
- 11 amdgpu_dm_crtc_atomic_check
- 12 amdgpu_dm_dc_clocks_state
- 13 amdgpu_dm_dce_clocks_state
- 14 amdgpu_dm_dc_pipe_state
- 15 amdgpu_dm_plane_atomic_check
- 16 amdgpu_dmub_trace_high_irq
- 17 **amdgpu_refresh_rate_track**
- 18 dcn_fpu
- 19 dcn_optc_lock_unlock_state

Checking the DTN log

[dtn begin]

HUBBUB WM:	data_urgent	pte_meta_urgent	sr_enter	sr_exit	dram_clk_change
WM_Set[0]:	8.500	0.000	56.000	19.360	412.500
WM_Set[1]:	8.500	0.000	56.000	19.360	412.500
WM_Set[2]:	8.500	0.000	56.000	19.360	46.500
WM_Set[3]:	8.500	0.000	56.000	19.360	412.500

HUBP:	format	addr_hi	width	height	rot	mir	sw_mode	dcc_en	blank_en	clock_en	ttu_dis	underflow	min_ttuvblank	qos_low_wm	qos_high_wm
[0]:	8h	80h	1920	2160	0h	0h	0h	0	0	1	0	0h	413.220	0.000	30.000
[1]:	0h	0h	0	0	0h	0h	0h	0	0	0	0	0h	0.000	0.000	0.000
[2]:	0h	0h	0	0	0h	0h	0h	0	0	0	0	0h	0.000	0.000	0.000
[3]:	0h	0h	0	0	0h	0h	0h	0	0	0	0	0h	0.000	0.000	0.000
[4]:	0h	0h	0	0	0h	0h	0h	0	0	0	0	0h	0.000	0.000	0.000
[5]:	8h	80h	1920	2160	0h	0h	0h	0	0	1	0	0h	413.220	0.000	30.000

UMR - Info

2.0 scale sienna_cichlid (instance: 0)			
info registers Waves Rings Power Memory Usage Top MS Memory Inspector			
ASIC name	sienna_cichlid		HW block names
Instance	0		df371
DID	73:bf		mp11107
Family	NV		mmhub210
VRAM	16368 MB		osssys503
Visible VRAM	256 MB		vcn301{1}
vBios version	113-1E4392U-05H		vcn300
Firmware	Feature version	Firmware version	clkbl1103
VCE	0x0	0x0	hdp503
UVD	0x0	0x0	smuio1106
MC	0x0	0x0	athub210
ME	0x2c	0x40	dcn300
PFP	0x2c	0x62	thm1105
CE	0x2c	0x25	mp01107
RLC	0x1	0x60	umc870{7}
RLC	0x0	0x0	umc870{5}
RLC	0x0	0x0	umc870{3}
RLC	0x0	0x0	umc870{1}
RLCP	0x0	0x0	umc870{6}
RLCV	0x0	0x0	umc870{4}
MEC	0x2c	0x76	umc870{2}
MEC2	0x2c	0x76	umc870{0}
IMU	0x0	0x0	gfx1030
SOS	0x0	0x210e64	clka1103{7}
ASD	0x210000de	0x210000de	clka1103{5}
TA	0x0	0x0	clka1103{3}
TA	0x0	0x0	clka1103{1}
TA	0x0	0x0	clka1103{8}
TA	0x0	0x0	clka1103{6}
TA	0x0	0x0	clka1103{4}
TA	0x0	0x0	clka1103{2}
SMC	0x0	0x0	clka1103{0}
SDMA0	0x34	0x53	clka1103{9}
SDMA1	0x34	0x53	Link Speed
SDMA2	0x34	0x53	16.0 GT/s PCIe
SDMA3	0x34	0x53	Link Width
VCN	0x0	0x411E000	x 16
DMCU	0x0	0x0	
DMCUB	0x0	0x2020020	
IOC	0x0	0x0	
1E4392U-05H	0x0	0x2d333131	
	0x0	0x0	

Repository: <https://gitlab.freedesktop.org/tomstdenis/umr>

UMR - Registers

2.0 | scale | sienna_cichlid (instance: 0)

Info Registers Waves Rings Power Memory Usage Top XMS Memory Inspector

dcn300 (6/8829 registers)

- mmHUBPRE00_DCSURF_SURFACE_CONTROL
- mmHUBPRE01_DCSURF_SURFACE_CONTROL
- mmHUBPRE02_DCSURF_SURFACE_CONTROL
- mmHUBPRE03_DCSURF_SURFACE_CONTROL
- mmHUBPRE04_DCSURF_SURFACE_CONTROL
- mmHUBPRE05_DCSURF_SURFACE_CONTROL

Filters

	Register name	Clear
PRIMARY_SURFACE_DCC_EN	Register field name	Clear

Register watchlist:

Auto-refresh

Pin Name	Address	Value	Bitfield	R	W
<input checked="" type="checkbox"/> mmHUBPRE00_DCSURF_SURFACE_CONTROL	0x00003ada	0x0000	PRIMARY_SURFACE_TMZ [0:0] 0x0 PRIMARY_SURFACE_DCC_EN [1:1] 0x1 PRIMARY_SURFACE_DCC_IND_BLK [3:2] 0x3 PRIMARY_SURFACE_TMZ_C [4:4] 0x0 PRIMARY_SURFACE_DCC_IND_BLK_C [6:5] 0x0 SECONDARY_SURFACE_TMZ [8:8] 0x0 SECONDARY_SURFACE_DCC_EN [9:9] 0x1 SECONDARY_SURFACE_DCC_IND_BLK [11:10] 0x3 SECONDARY_SURFACE_TMZ_C [12:12] 0x0 SECONDARY_SURFACE_DCC_IND_BLK_C [14:13] 0x0 PRIMARY_META_SURFACE_TMZ [16:16] 0x0 PRIMARY_META_SURFACE_TMZ_C [17:17] 0x0 SECONDARY_META_SURFACE_TMZ [18:18] 0x0 SECONDARY_META_SURFACE_TMZ_C [19:19] 0x0		

Repository: <https://gitlab.freedesktop.org/tomstdenis/umr>

UMR - Power

2.0 | scale sienna_cichlid (instance: 0)

info registers waves Rings power Memory Usage top MS Memory Inspector

Select DPM profile :

- auto
- low
- high
- manual
- profile_standard
- profile_min_sclk
- profile_min_mclk
- profile_peak

Sensors values:

0.5 sec Refresh interval (drag to modify)

GFX_SCLK : 23 MHz

GFX_MCLK : 456 MHz

AVG_GPU : 19 W

GPU_LOAD : 3 %
MEM_LOAD : 2 %

PowerPlay features:

<input checked="" type="checkbox"/> DPM_PREFETCHER	<input checked="" type="checkbox"/> DPM_GFXCLK
<input checked="" type="checkbox"/> DPM_GFX_GPO	<input checked="" type="checkbox"/> DPM_UCLK
<input checked="" type="checkbox"/> DPM_FCLK	<input checked="" type="checkbox"/> DPM_SOCCLK
<input checked="" type="checkbox"/> DPM_MP8CLK	<input checked="" type="checkbox"/> DPM_LINK
<input checked="" type="checkbox"/> DPM_DCEFCLK	<input checked="" type="checkbox"/> DPM_XGMI
<input checked="" type="checkbox"/> MEM_VDDCI_SCALING	<input checked="" type="checkbox"/> MEM_MVDD_SCALING
<input checked="" type="checkbox"/> DS_GFXCLK	<input checked="" type="checkbox"/> DS_SOCCLK
<input checked="" type="checkbox"/> DS_FCLK	<input checked="" type="checkbox"/> DS_LCLK
<input checked="" type="checkbox"/> DS_DCEFCLK	<input checked="" type="checkbox"/> DS_UCLK
<input checked="" type="checkbox"/> GFX_ULV	<input checked="" type="checkbox"/> FW_DSTATE
<input checked="" type="checkbox"/> GFXOFF	<input checked="" type="checkbox"/> BACO
<input checked="" type="checkbox"/> MM_DPM_PG	<input checked="" type="checkbox"/> TDC
<input checked="" type="checkbox"/> PPT	<input checked="" type="checkbox"/> GTHR
<input checked="" type="checkbox"/> APCC_PLUS	<input checked="" type="checkbox"/> VR0HOT
<input checked="" type="checkbox"/> ACDC	<input checked="" type="checkbox"/> FW_CTF
<input checked="" type="checkbox"/> VR1HOT	<input checked="" type="checkbox"/> THERMAL
<input checked="" type="checkbox"/> FAN_CONTROL	<input checked="" type="checkbox"/> RM
<input checked="" type="checkbox"/> GFX_DCS	<input checked="" type="checkbox"/> GFX_SS
<input checked="" type="checkbox"/> LED_DISPLAY	<input checked="" type="checkbox"/> TEMP_DEPENDENT_VMIN
<input checked="" type="checkbox"/> OUT_OF_BAND_MONITOR	<input checked="" type="checkbox"/> ATHUB_PG
<input checked="" type="checkbox"/> MMHUB_PG	
<input checked="" type="checkbox"/> APCC_DFLI	
<input checked="" type="checkbox"/> RSMU_SMN_CG	

hwmon0:

Fan:

0 % Control Mode: auto manual (1)

Temperatures:

Label	Value (°C)	Critical (°C)
edge	38	100
junction	41	110
mem	40	100

Repository: <https://gitlab.freedesktop.org/tomstdenis/umr>

UMR - KMS

2.0 | scale sienna_cichlid (instance: 0)

Info Registers Waves Rings Power Memory Usage Top KMS Memory Inspector

KMS plane visual indicator: Refresh Auto-refresh: Interval: 0.5 sec

Framebuffers Planes CRTCs Connectors

[fbcon]

- id: 130
 - format: XR24 little-endian
 - fourcc: 0x34325258
 - modifier: 0x0
 - size: 3840x2160
 - Layers
 - size: 3840x2160
 - pitch: 15360

Xorg

- id: 151
- id: 152
- id: 164
- id: 167
 - format: AR24 little-endian
 - fourcc: 0x34325241
 - modifier: 0x0
 - size: 256x256
 - Layers
 - size: 256x256
 - pitch: 1024

Planes

- id: 0
- id: 1
- id: 2
- id: 3
- id: 4
- id: 5 w: 3840 h: 2160 fb: 152
- id: 6
- id: 7
- id: 8 w: 256 h: 256 fb: 167
- id: 9
- id: 10
- id: 11
- id: 12
- id: 13

CRTCs

- id: 0
 - enable: 1
 - active: 1
 - dcc: on
 - tmz: off
- id: 1
 - enable: 0
 - active: 0
- id: 2
 - enable: 0
 - active: 0
- id: 3
 - enable: 0
 - active: 0
- id: 4
 - enable: 0
 - active: 0
- id: 5
 - enable: 0
 - active: 0

Connectors

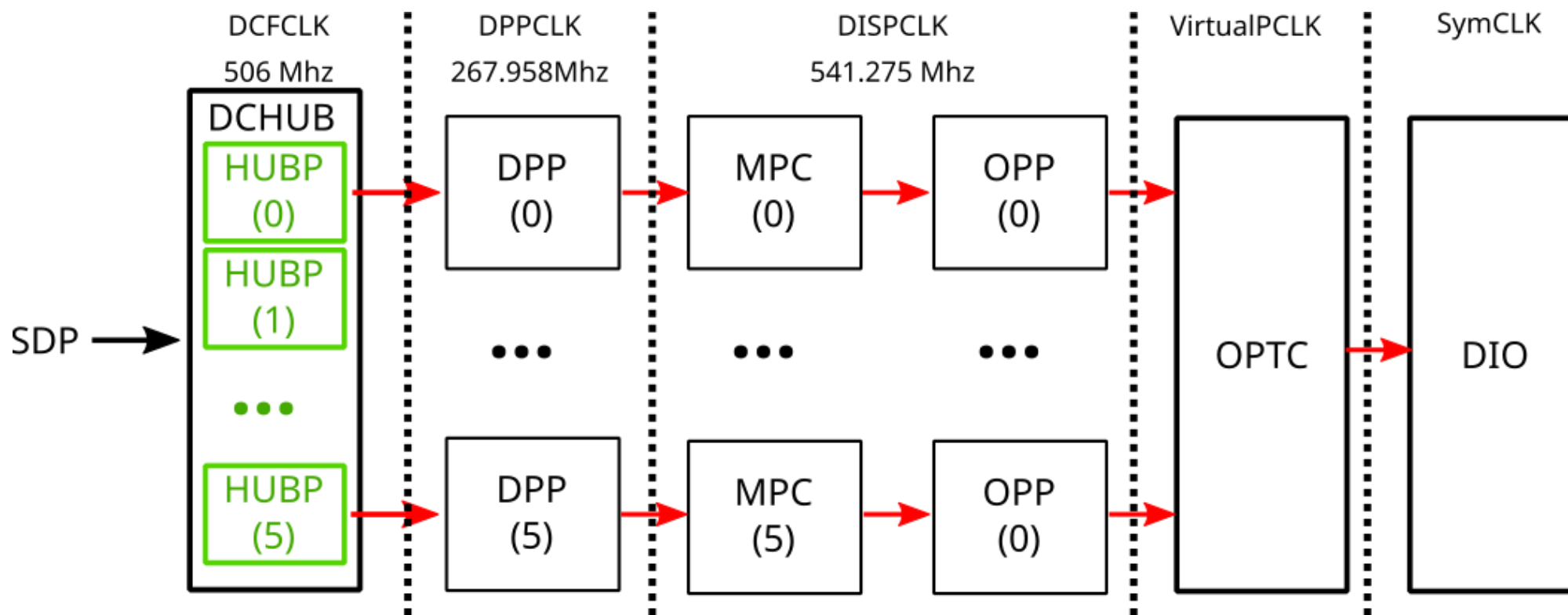
- DP-1
- DP-2
- DP-3
- HDMI-A-1
- Writeback-1

Repository: <https://gitlab.freedesktop.org/tomstdenis/umr>



Specific debugs

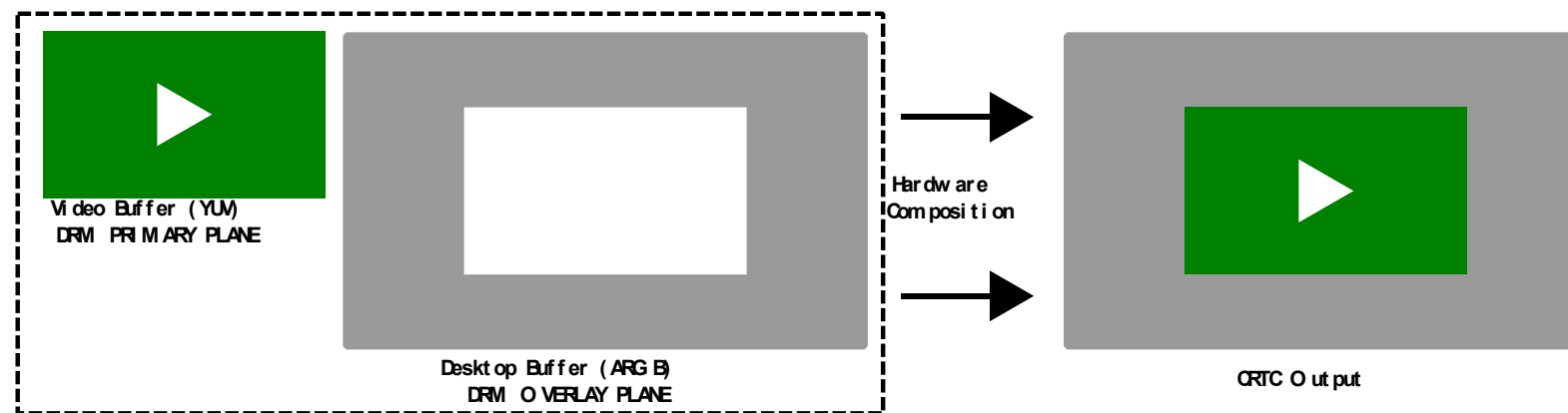
Pipe Split



Ref:

- <https://www.kernel.org/doc/html/latest/gpu/amdgpu/display/dcn-overview.html>

Pipe Split - MPO

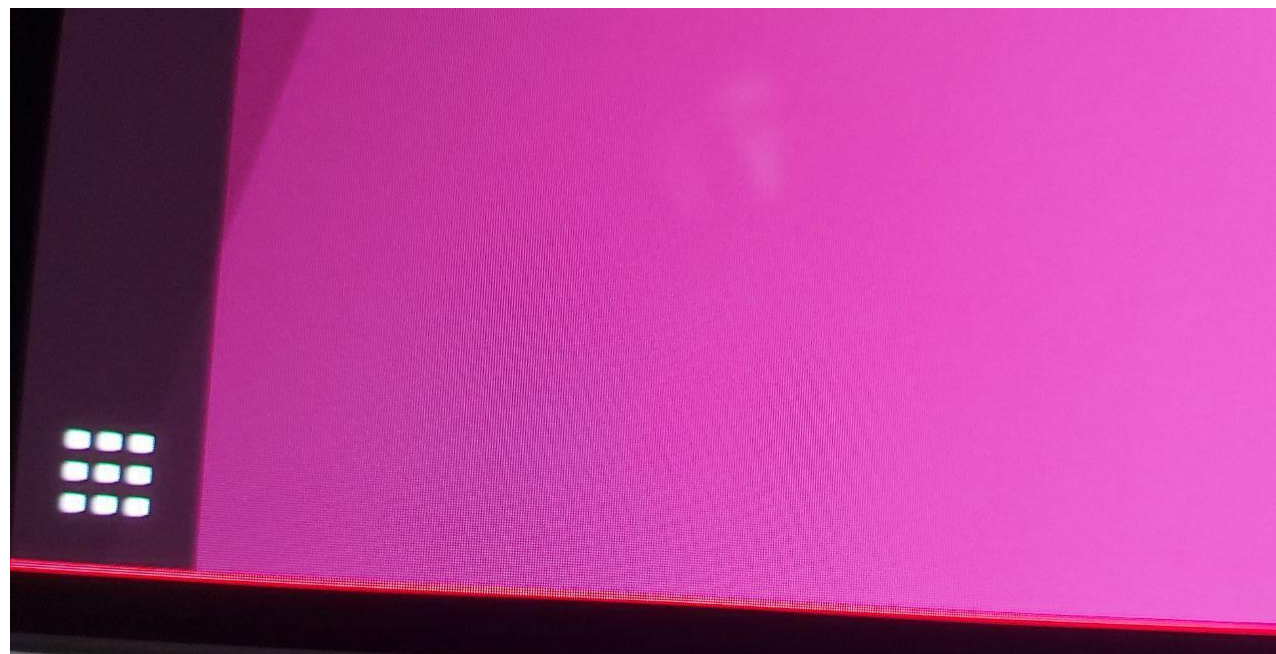
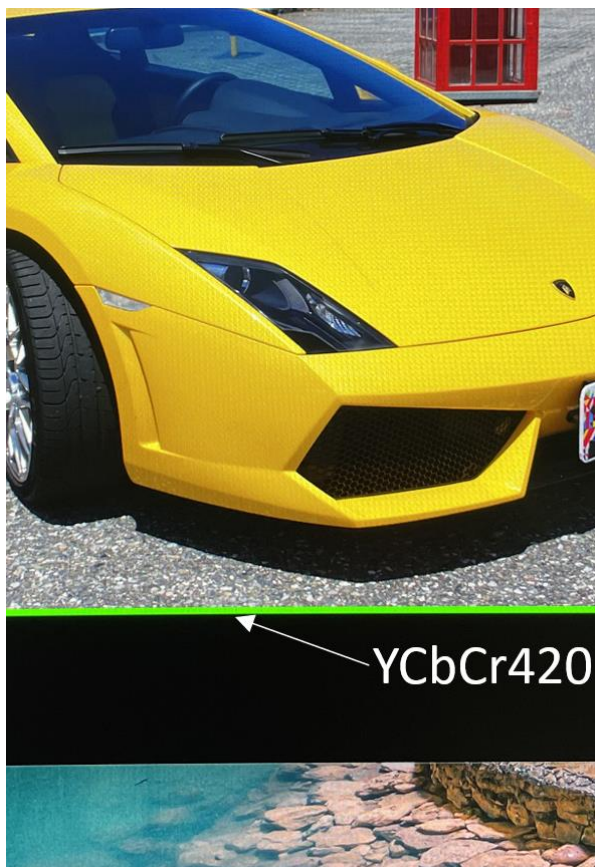


Ref:

- <https://www.kernel.org/doc/html/latest/gpu/amdgpu/display/mpo-overview.html>

Pipe Split - Visual confirm

```
echo 1 > /sys/kernel/debug/dri/0/amdgpu_dm_visual_confirm
```



Horizontal Glitches

When it might happen:

- High-resolution displays with a high refresh rate.
- Multiple displays.

Check if it is a clock issue by increasing the power usage:

```
bash -c "echo high > /sys/class/drm/card0/device/power_dpm_force_performance_level"
```


Horizontal Glitches

In a dGPU with a display that supports a high refresh rate, try to disable SubVP or FAMS:

```
struct dc debug options {
    bool native422_support;
    bool disable_dsc;
    enum visual_confirm visual_confirm;
    int visual_confirm_rect_height;

    bool sanity_checks;
    bool max_disp_clk;
    bool surface_trace;
    bool timing_trace;
    bool clock_trace;
    bool validation_trace;
    bool bandwidth_calcs_trace;
    int max_downscale_src_width;

    bool disable_fams;
    enum in_game_fams_config disable_fams_gaming;
    /* FEC/PSR1 sequence enable delay in 100us */
    uint8_t fec_enable_delay_in100us;
    bool enable_driver_sequence_debug;
    enum det_size crb_alloc_policy;
    int crb_alloc_policy_min_disp_count;
    bool disable_z10;
    bool enable_z9_disable_interface;
    bool psr_skip_crtc_disable;
    uint32_t ips_skip_crtc_disable_mask;
    union dpia_debug_options dpia_debug;
    bool disable_fixed_vs_aux_timeout_wa;
    uint32_t fixed_vs_aux_delay_config_wa;
    bool force_disable_subvp;
```

AMD 

IGT

IGT Tests

tast.graphics.IGT.drm_import_export	1	1	1	1
tast.graphics.IGT.drm_mm	1	1	1	1
tast.graphics.IGT.drm_read	1	1	1	1
tast.graphics.IGT.kms_addfb_basic	1	1	1	1
tast.graphics.IGT.kms_atomic	1	1	1	1
tast.graphics.IGT.kms_atomic_interruptible	1	1	1	1
tast.graphics.IGT.kms_atomic_transition	1	1	1	1
tast.graphics.IGT.kms_big_fb	1	1	1	1
tast.graphics.IGT.kms_concurrent	1	1	1	1
tast.graphics.IGT.kms_draw_crc	1	1	1	1
tast.graphics.IGT.kms_getfb	1	1	1	1
tast.graphics.IGT.kms_hdmi_inject	1	1	1	1
tast.graphics.IGT.kms_hdr	1	1	1	1
tast.graphics.IGT.kms_plane	1	1	1	1
tast.graphics.IGT.kms_plane_cursor	1	1	1	1
tast.graphics.IGT.kms_plane_lowres	1	1	1	1
tast.graphics.IGT.kms_prime	1	1	1	1
tast.graphics.IGT.kms_prop_blob	1	1	1	1
tast.graphics.IGT.kms_properties	1	1	1	1
tast.graphics.IGT.kms_rmfb	1	1	1	1
tast.graphics.IGT.kms_universal_plane	1	1	1	1
tast.graphics.IGT.sw_sync	1	1	1	1
tast.graphics.IGT.testdisplay	1	1	1	1
tast.graphics.IGT.vgem_basic	1	1	1	1
tast.graphics.IGT.vgem_slow	1	1	1	1

tast.graphics.IgtAmdgpu.amd_basic	48	14		70
tast.graphics.IgtAmdgpu.amd_bypass	6			
tast.graphics.IgtAmdgpu.amd_color				1
tast.graphics.IgtAmdgpu.amd_cp_dma_misc	48	14		70
tast.graphics.IgtAmdgpu.amd_cs_nop	48	14	35	69
tast.graphics.IgtAmdgpu.amd_deadlock	48			
tast.graphics.IgtAmdgpu.amd_dp_dsc		14	35	4
tast.graphics.IgtAmdgpu.amd_hotplug	4			2
tast.graphics.IgtAmdgpu.amd_llr	48	14		66
tast.graphics.IgtAmdgpu.amd_info		14	35	66
tast.graphics.IgtAmdgpu.amd_link_settings			35	4
tast.graphics.IgtAmdgpu.amd_mode_switch	6		35	67
tast.graphics.IgtAmdgpu.amd_module_load	48	14	35	70
tast.graphics.IgtAmdgpu.amd_pci_unplug			34	
tast.graphics.IgtKms.kms_addfb_basic		14	35	70
tast.graphics.IgtKms.kms_atomic	68	1		
tast.graphics.IgtKms.kms_atomic_interruptible	68	16	32	85
tast.graphics.IgtKms.kms_atomic_transition			35	67
tast.graphics.IgtKms.kms_color	42	14	3	70
tast.graphics.IgtKms.kms_concurrent	6		35	67
tast.graphics.IgtKms.kms_cursor_legacy	16			6
tast.graphics.IgtKms.kms_flip	16	1	7	11
tast.graphics.IgtKms.kms_flip_event_leak	6		35	67
tast.graphics.IgtKms.kms_getfb	48	14	35	70
tast.graphics.IgtKms.kms_pipe_crc_basic	6	6	1	64
tast.graphics.IgtKms.kms_plane_alpha_blend				47
tast.graphics.IgtKms.kms_plane_scaling_unstable	6		34	3
tast.graphics.IgtKms.kms_prop_blob	48	14	34	70
tast.graphics.IgtKms.kms_properties	48	14	34	70
tast.graphics.IgtKms.kms_rmfb	6		34	67
tast.graphics.IgtKms.kms_rotation_crc			2	1
tast.graphics.IgtKms.kms_setmode	6		34	4
tast.graphics.IgtKms.kms_sysfs_edid_timing	48	14	34	70
tast.graphics.IgtKms.kms_universal_plane	6			
tast.graphics.IgtKms.kms_vblank	16	5	12	17
tast.graphics.IgtKms.kms_vrr	6		34	67



Contribute to Display Code

Consider to Contribute to Display

AMDGPU - Display Contributions ¶

First of all, if you are here, you probably want to give some technical contribution to the display code, and for that, we say thank you :)

This page summarizes some of the issues you can help with; keep in mind that this is a static page, and it is always a good idea to try to reach developers in the amdgfx or some of the maintainers. Finally, this page follows the DRM way of creating a TODO list; for more information, check [‘TODO list’](#).

Ref: <https://www.kernel.org/doc/html/latest/gpu/amdgpu/display/display-contributing.html>

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