

Fast gfx in a vm with this one little trick!

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- Device Emulation
- API Remoting
- Fixed Passthrough
- Mediated Passthrough

- Device Emulation
  - Are you kidding?
- API Remoting
- Fixed Passthrough
- Mediated Passthrough

- Device Emulation
- API Remoting
  - le, virgl, gfxstream, venus
  - 12-86% of native
  - Isolation?
- Fixed Passthrough
- Mediated Passthrough

- Device Emulation
- API Remoting
- Fixed Passthrough
  - le. PCI passthrough
  - Near native perf
  - $\circ$   $\,$  Not useful if host and other VMs also need same GPU  $\,$
- Mediated Passthrough

- Device Emulation
- API Remoting
- Fixed Passthrough
- Mediated Passthrough
  - Great... if your hw supports it
  - Fence/buffer integration with host?

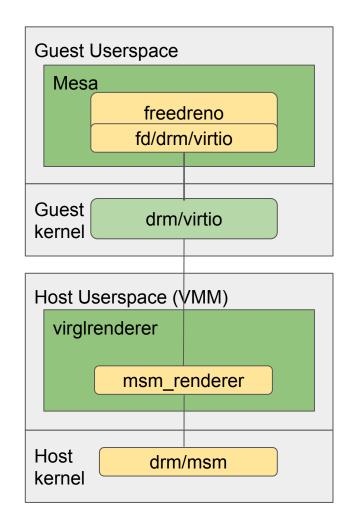


- Aka virtio\_gpu aka drm/virtio
  - Upstream virtio based guest kernel vgpu driver
- Host/guest interop
- Recent(ish) additions
  - Blob resources
  - Context Type
  - $\circ$  Ring-idx

Guest Userspace
Mesa
virgl venus
Guest drm/virtio
Host Userspace (VMM) virglrenderer
vrendvkr
gl vk
Host drm/\$driver kernel

# ORM Native Context!

- Native usermode driver in guest!
- API remoting at kernel uabi layer
  - Level of least frequent calls
  - And least frequent change
  - Make it more async!
- Hooks in at src/freedreno/drm
  - Basically equiv of winsys layer
- Integrates with virtgpu's buffer/fence passing
- Not much code
  - < 2kloc guest userspace</li>
  - ~ 1.3kloc in virglrenderer



#### Virtgpu DRM Native Context: Structure

#### • Device fd's (virglrenderer):

- 1 device fd (struct drm\_file \*) per guest process
- Guest drm\_file 1:1 with host virglrenderer context
- Virglrenderer context 1:1 with host drm\_file
- GPU address spaces are 1:1 with drm\_file
- One GPU address space per guest process
- GEM:
  - 1:1 between host and guest (plus shmem buffer)
  - All host-storage blob's (VIRTGPU\_RESOURCE\_CREATE\_BLOB)

# Virtgpu DRM Native Context: Fences/Sync

- ring\_idx == 0: The CPU timeline
  - Used in cases where guest needs to wait for host CPU
- ring\_idx > 0: Maps 1:1 to GPU priority levels
  - Which map 1:1 to host dma-fence contexts / timelines
- res\_id handles passed to VIRTGPU\_EXECBUFFERioctl
- Synchronization in guest
  - Don't block in host VMM
  - TODO virtgpu needs proto to pass host fences from guest

# Virtgpu DRM Native Context: Protocol

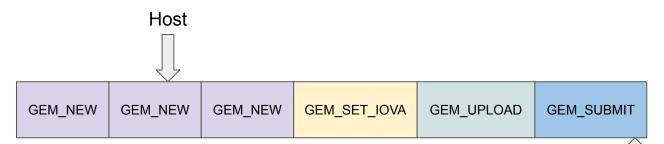
- Guest  $\rightarrow$  Host: VIRTGPU\_EXECBUFFER
  - Req messages tunneled over EB
  - Batching for async requests
- $\bullet \quad \text{Host} \to \text{Guest: shmem buffer}$ 
  - Rsp messages written into shmem rsp\_mem buffer at offset guest asks for
  - Keeps the design/implementation of host VMM simple

# Virtgpu DRM Native Context: Protocol

- Keep it asynchronous!!
  - To mitigate host ⇔ guest latency, keep hot-paths async
- Host uapi additions to support this
  - Userspace allocated GPU virtual address GEM create/import can be async
  - Seqno fence # assignment in userspace GEM submit can be async
- Treat errors as context-lost

# Virtgpu DRM Native Context: Protocol

• Keep it asynchronous!! Simple Example:



- Guest allocates 3 buffers (NEW), imports 1 (SET\_IOVA)
  - GPU VA passed from guest userspace
  - Guest kernel res\_id used instead of host allocated handle in proto

Guest

- UPLOAD can avoid mmap into host or immediate mmap
  - Guest mmap requires host to have actually allocated the BO

#### Alternatives? rendernode fwding?

- Rendernode device exposed in guest
  - Fwd (modern subset) of ioctls to host
  - Use unmodified mesa in guest
- Too synchronous!
  - loctls return a value + \_IOC\_READ
  - Existing uapi designed around low syscall cost
  - Better to embrace the async!



- Virglrenderer:
  - <u>src/drm/msm/msm\_proto.h</u> the guest ⇔ host protocol
  - <u>src/drm/msm/msm\_renderer.c</u> one .c file, ~1.3kloc
  - <u>src/drm</u> helper to deal with fences, simple driver loader
- mesa:
  - o <u>src/freedreno/drm/virtio</u>

# Adding your driver in three easy steps (1/3)

• Step #1 – add context id and extend capset (<u>drm\_hw.h</u>):

```
struct virgl_renderer_capset_drm {
   uint32 t wire format version;
   /* Underlying drm device version: */
   uint32 t version major;
   uint32 t version minor;
   uint32 t version patchlevel;
#define VIRTGPU DRM CONTEXT MSM 1
   uint32 t context type;
   uint32 t pad;
   union {
      struct {
         uint32 t has cached coherent;
         . . .
      } msm; /* context type == VIRTGPU DRM CONTEXT MSM */
   } u;
};
```

# Adding your driver in three easy steps (2/3)

- Step #2 ???
  - Define and implement your own protocol
  - Then add yourself to the loader table in <u>drm\_renderer.c</u>:

```
static const struct backend {
   uint32 t context type;
   const char *name;
   int (*probe)(int fd, struct virgl renderer capset drm *capset);
   struct virgl context *(*create)(int fd);
} backends[] = {
#ifdef ENABLE DRM MSM
   ł
      .context type = VIRTGPU DRM CONTEXT MSM,
      .name = "msm",
      .probe = msm renderer probe,
      .create = msm renderer create,
   },
#endif
};
```

#### Adding your driver in three easy steps (3/3)

• Step #3 – Profit!



#### • Possible optimizations:

- Fencing improvements in virtgpu pass host fences back to host
- $\circ \quad \text{Reduce host} \to \text{guest fence latency}$
- Virtgpu drm\_syncobj support
- QEMU support



Questions?