Results of BVH building break-out with RADV

The good news is code sharing looks possible but...

- It's unclear how command-streamer control-flow will work on AMD
- RADV may need to kick off compute shaders for ALU stuff
- GRL -> NIR is looking likely but details TBD.
- Need to generalize things a bit
  - AMD has its own BVH format (new AMD back-end)
  - AMD BVHs are 4-ary as opposed to 6-ary on Intel
  - Likely means the sorting algorithms will need to be generalized
- Next step is for Intel folks to post GRL code so Bas can play with it