etnaviv status update

2021

whoami

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Long term etnaviv developer

my personal views and toughs

Overview

Overview

etnaviv is an open source graphics driver which supports embedded GPUs from Vivante via reverse engineering

Upstreamed in mesa 17.0

- GC600 (STMicroelectronics STM32MP157C)
- GC860 (Ingenic JZ4770 MIPS: GCW Zero)
- GC880 (Freescale i.MX 6 DualLite)
- GC2000 (Freescale i.MX 6 Quad)
- GC3000 (Freescale i.MX 6 Quad Plus)
- GC7000L (Freescale i.MX 8 M)

and many more...

State

It's not easy..

State

no documentation

not that many developers - sadly

not much interest from companies

just an other hobby

State

Nevertheless there was some work done during the last year

State

kernel side

- mmu fixes - thanks Lucas
- new hwdb for some GC7000 models
- basic maintenance

State

mesa side

- drm-shim support
- shader cache support
- NTE support
- fixes all over the place
- basic maintenance
- NIR stuff

CI

CI

more testing for patches is needed

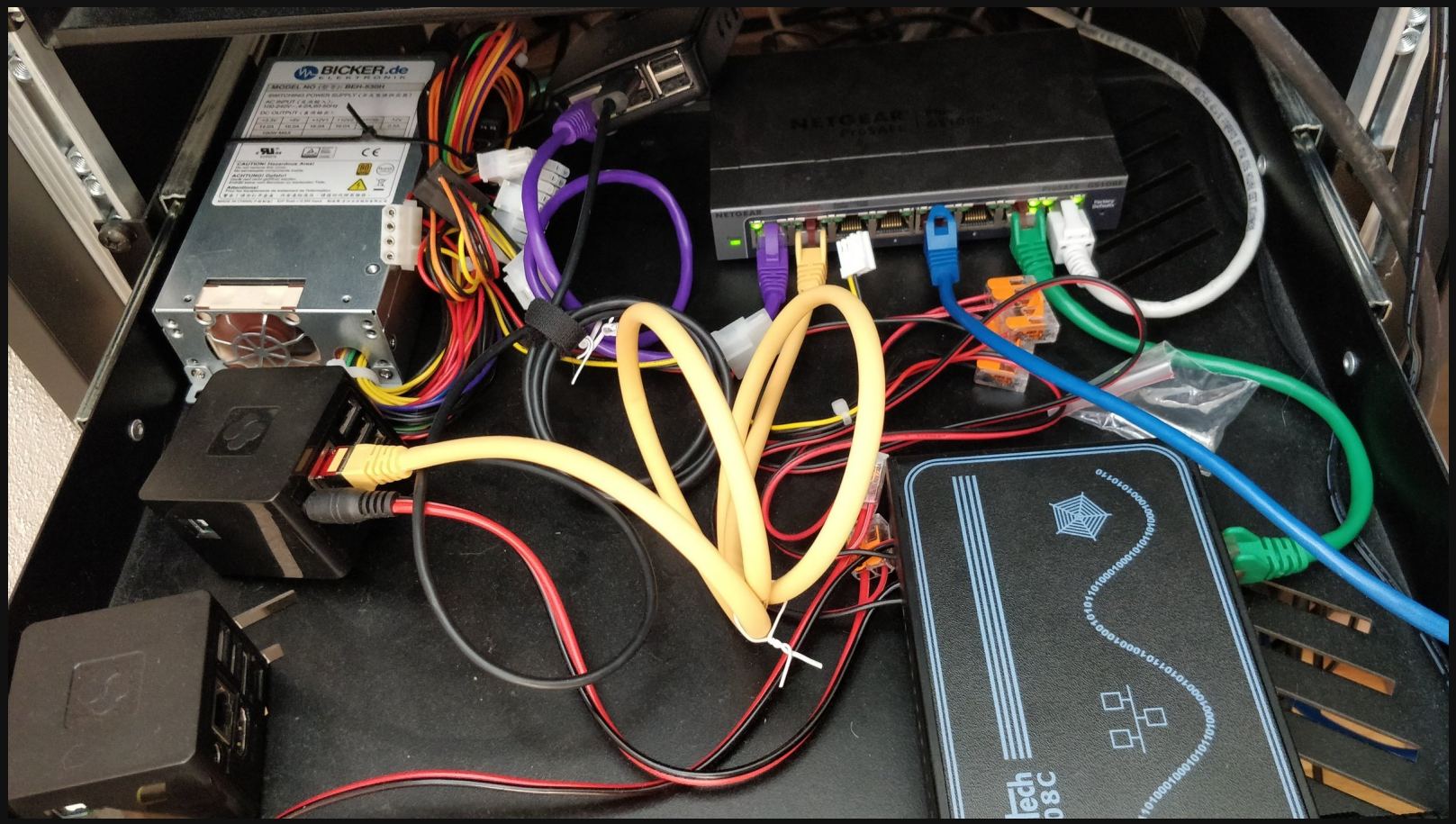
baremetal based

unraid based NAS for gitlab-runner

ser2net for console logging (rpi)

eth based power control

CI



CI

what is missing to go live?

nothing \o/

MR 12852

NIR

NIR

author of nir compiler is not active anymore

maintenance quite hard

nir validation problems

cleanup and refactoring work started

NIR

refactoring process

- capture generated shader code with stats (shader-db)
- do a 'simple' refactoring step
- figure our what went wrong
- write unit tests to keep it working over time
- run deqp/piglit

NIR

lot of cleanup's landed

lot of crash fixes landed

rect texture lowering moved to st (vc4 uses it too)

some compiler opts landed

time to make it the default

isaspec

isaspec

ISASPEC - XML Based ISA Specification

isaspec provides a mechanism to describe an instruction set in xml, and generate a disassembler and assembler (eventually). The intention is to describe the instruction set more formally than hand-coded assembler and disassembler, and better decouple the shader compiler from the underlying instruction encoding to simplify dealing with instruction encoding differences between generations of GPU.

Benefits of a formal ISA description, compared to hand-coded assemblers and disassemblers, include easier detection of new bit combinations that were not seen before in previous generations due to more rigorous description of bits that are expect to be '0' or '1' or 'x' (dontcare) and verification that different encodings don't have conflicting bits (ie. that the specification cannot result in more than one valid interpretation of any bit pattern).

- Maximum "bitset" size is 64b
- Fixed instruction size

MR 11321

Future

Future

finish NIR translation

GLES3 support

fixing broken stuff on different GPUs

Thank you!

#etnaviv @ OFTC